

Non-stall Pipeline Microprocessor

## ABSTRACT

Sub A2

5 A method of executing microprocessor instructions and an associated microprocessor are disclosed. Initially, a conditional branch instruction is fetched from a storage unit such as an instruction cache. Branch prediction information embedded in the branch instruction is detected by a fetch unit of the microprocessor. Depending upon the state of the branch prediction information, instructions from the branch-taken path and the branch-not-taken path of the branch  
10 instruction are fetched. The branch-not-taken path instructions and the branch-taken path instruction may be speculatively executed. Upon executing the conditional branch instruction, the speculative results from the branch-taken path are discarded if the branch is not taken and speculative results from the branch-not-taken path are discarded if the branch is taken. The branch prediction information may include compiler generated information indicative of the context in which the conditional branch instruction is used. In one embodiment, the branch prediction information causes instruction fetching from both the taken and non taken branches if the compiler determines the branch instruction to unpredictable. In another embodiment, fetching instructions from the branch-taken path includes fetching a predetermined number of instructions from the branch-taken path and a predetermined number of instructions from the  
20 branch-not-taken path. In another embodiment, instructions are fetch down the branch-not-taken path until a subsequent branch instruction is encountered.